REMARKS

Claims 1-24 are currently pending.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and receipt of the priority document.

35 U.S.C. §103

Claims 1-9 stand rejected as being unpatentable over Thompson et al, U.S. Patent No. 6,510,309 in view of Tanaka (JP 57-43453). Further, claims 10-14 and 15-21 are rejected as being unpatentable over the Thompson and Tanaka combination in view of Lysejko et al., U.S. Patent No. 6,298,246, and further in view of Yamamoto et al, U.S. Patent No. 6,308,047 (claim 14 only). Reconsideration of the rejections is requested for the following reasons.

Independent claim 1 has been amended to include that none of the wirings are arranged to traverse the wirings connected between the first electrode terminal and the first electrode of the transistor, between the second electrode terminal and the second electrode of the transistor, and between the third

electrode terminal and the control electrode of the transistor. For example, with reference to Fig. 6, none of the wirings traverse the wirings 120c, 120b and 120a between electrode terminals 101, 102, 103 and the electrode terminals 12C, 14C and 13C of the transistor 110. Independent claim 10 has been similarly amended with respect to wirings connected, for example, between the electrode terminals 101, 205 and the first electrodes of the transistors 110, 111, between the electrode terminals 102, 206 and the second electrodes of the transistors 110, 111, and between the electrode terminals 103, 207 and the control electrodes of the transistors 110, 111. As amended, the independent claims are patentable over the combination of Thompson and Tanaka.

In the present invention, the layout of the system components is configured to suppress parasitic inductance. As shown in Fig. 1, the leads 201-209 are connected with electrode terminal pads 101-109 through conductive wires 211. As shown in Fig. 3, the low-noise amplifier 210 is connected to the pads 212 to which the conductive wires are connected. No wires are shown between the edge 119 of the semiconductor chip 313 and the electrode terminals 101-109. Further, no

wiring traverses the wires connected between the electrode terminal 101 and an output electrode of low-noise amplifier 110, between the electrode terminal 102 and a ground electrode of the low-noise amplifier 110 and between the electrode terminal 103 and a control electrode of the low-noise amplifier 110, except for the wires connected between the electrostatic discharge protecting circuits 110, 113 and 114 and control electrodes of the low-noise amplifier. The significance of these arrangements is discussed in the specification, for example, *see* page 18, line 21 to page 20, line 3.

Thompson discloses an amplifying circuit including a filter 38 commonly used between the reception circuit and a transmission circuit, and amplifiers connected to one and the other sides of the filter. A switch circuit is also provided on the input of amplifier CA1. Further, a switch circuit is provided on the output of amplifier CA2, switching between transmission and reception. Thompson is relied upon for showing no wiring traversing the wires connected between the pads and amplifiers, as shown in Figs. 3, 4 and 5 of the reference.

However, Figs. 3-5 of Thompson are circuit diagrams, not layout drawings of the components and wirings. The reference does not shown the layout of pads and amplifiers arranged on a semiconductor chip, and therefore the drawings do not show the wirings claimed by Applicants. Specifically, Figs. 3-5 of Thompson do not illustrate the absence of wires traversing the wires connecting between the pads and the amplifiers.

Tanaka discloses a differential amplifier formed on a semiconductor chip on which pads are arranged for the collector, base and emitter of the transistors. The pads 1, 2, 3, 6 and 7 are connected to the collectors, bases and emitters and are arranged along an edge portion or the chip edge of the semiconductor chip 8. As shown in Fig. 3 of Tanaka, the pads 3, 6 and 7 are also arranged near or around the center of the semiconductor chip. However, Tanaka does not describe or disclose the pads being arranged near the chip or near the center of the chip for the reasons set forth by Applicants. Accordingly, there is no teaching to one having ordinary skill in the art of combining Tanaka and Thompson in the manner suggested in the Office Action.

Although Yamamoto and Lysejko are relied upon in rejection of dependent claims, neither of these references overcomes the deficiencies of Thompson and Tanaka. Accordingly, the independent claims are patentable over the art of record and the dependent claims should also be found to be patentable over the art of record at least for depending from an allowable independent claim.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination is requested.

Respectfully submitted,

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